Exams: **Introduction to Semiconductor Devices (191217061)**
Date: **Wednesday, 16-04-2014**
Time: **13:45-17:15 for full exams*)**
Location: **Sportcentrum**

This exams comprises 4 parts:

Semiconductor physics	Question 1
PN-junction	Question 2
Bipolar Junction Transistor	Question 3
MOS Transistor	Question 4

Students who passed the WASP test during the course of 2013/14 are allowed to skip question 2. In that case only questions 1, 3 and 4 will be counted for the final grade of the exams.

A calculator may be used during the exams, however it is **no** open book exams.

You are kindly requested to write down your name and student number on the forms.

Available time for the exams:

In case 3 questions are done:	3 hours till 16.45h
In case 4 questions are done:	3.5 hours till 17.15h

Attachment: Constants and equations sheet for semiconductor device physics.

Success!!!

Constants and equations Semiconductor Device Physics

Elementary charge:	$q=1.6\cdot10^{-19}\ C$
Thermal voltage equivalent (@ room temperature):	$u_T=kT/q=0.025\ V$
Dielectric constant (permittivity) Silicon:	$\varepsilon_{Si}=10^{-12}\ F/cm$
Dielectric constant (permittivity) Silicon dioxide:	$\varepsilon_{ox}=3.5\cdot10^{-13}\ F/cm$
Intrinsic carrier concentration (if not given):	$n_i=\sqrt{2}\cdot10^{10}\ cm^{-3}$
Electron diffusion constant (if not given):	$D_n=30\ cm^2/s$
Hole diffusion constant (if not given):	$D_p=10\ cm^2/s$
Electron mobility (if not given):	$\mu_n=1200\ cm^2/Vs$
Hole mobility (if not given):	$\mu_p=350\ cm^2/Vs$

1. **Semiconductor Physics** (spatially in one dimension)

Fermi-Dirac distribution

$$f(E)=\frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)}$$

Density of states (if not given)

$$g(E)\sim10^{47}\sqrt{E}$$

Carrier concentrations

$$n=N_C\exp\left(\frac{E_F-E_C}{kT}\right)=n_i\exp\left(\frac{E_F-E_{FI}}{kT}\right)$$

$$p=N_V\exp\left(\frac{E_V-E_F}{kT}\right)=n_i\exp\left(\frac{E_{FI}-E_F}{kT}\right)$$

Electrostatic potential

$$\psi=-\frac{E_{FI}}{q}$$

Fermi potential

$$\varphi_F=-\frac{E_F}{q}$$

General formalism

$$n=n_i\exp\left(\frac{\psi-\varphi_F}{u_T}\right)$$

$$p=n_i\exp\left(\frac{\varphi_F-\psi}{u_T}\right)$$

Current equations

$$j_n=qn\mu_n\mathcal{E}+qD_n\frac{dn}{dx}=n\mu_n\frac{dE_{FN}}{dx}$$

$$j_p=qp\mu_p\mathcal{E}-qD_p\frac{dp}{dx}=p\mu_p\frac{dE_{FP}}{dx}$$

Einstein relation

$$D=u_T\cdot\mu=\frac{kT}{q}\cdot\mu$$

Excess recombination rate (electrons)

$$R=\tilde{n}N_tc_n=\tilde{n}N_tv_{th}\sigma_n=\frac{\tilde{n}}{\tau_n}$$

Continuity equation (electrons)

$$\frac{d\tilde{n}}{dt} = \frac{1}{q}\frac{dj_n}{dx} - (R - G) = D_n \frac{d^2\tilde{n}}{dx^2} - \frac{\tilde{n}}{\tau_n}$$

Excess carrier diffusion (electrons)

$$\tilde{n}(x) = \tilde{n}_0 \exp\left(-\frac{x}{L_n}\right)$$

$$L_n = \sqrt{D_n \tau_n}$$

Poisson's equation

$$-\frac{d^2\psi(x)}{dx^2} = \frac{d\mathcal{E}(x)}{dx} = \frac{\rho(x)}{\varepsilon_s}$$

2. pn junction

Built-in potential

$$\phi_{bi} = u_T \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

Depletion layer width

$$W = \sqrt{\left(\frac{2\varepsilon_s (N_A + N_D)}{q N_A N_D}(\phi_{bi} - V_A)\right)}$$

Junction current (Shockley eq.) long diode

$$I = A(j_n + j_p) = -Aqn_i^2\left(\frac{D_n}{N_A L_n} + \frac{D_p}{N_D L_p}\right)\left(\exp\left(\frac{V_A}{u_T}\right) - 1\right)$$

Gummel number

$$G = \int_0^L \frac{N(x)}{D(x)} dx$$

Diffusion capacitance

$$C_{diff} = \frac{1}{u_T}(\tau_n j_n + \tau_p j_p) \approx \frac{\tau}{u_T} j$$

3. Bipolar transistor

Current density (NPN)

$$j = -\frac{qn_i^2}{G}\left(\exp\left(\frac{V_{BE}}{u_T}\right) - 1\right)$$

Definitions

$$I_E = -(I_B + I_C)$$

$$\beta_F = \frac{I_C}{I_B}$$

Small signal model

$$i_B = g_\pi v_{BE} + g_\mu v_{BC}$$

$$i_C = g_m v_{BE} + g_0 v_{BC}$$

4. MOS transistor

Charge storage

$$Q_n = -C_{ox}(V_{GB} - V_T)$$

Threshold voltage NMOS

$$V_T = V_{FB} + (2\phi_B + V_{SB}) + \frac{\sqrt{(2q\varepsilon_s N_A(2\phi_B + V_{SB}))}}{C_{ox}}$$

Drain current NMOS (strong inversion)

$$I_D = \frac{\mu_n C_{ox} W}{L}\left[\left(V_{GS} - 2\phi_B - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2\gamma}{3}\left\{(V_{SB} + 2\phi_B + V_{DS})^{1.5} - (V_{SB} + 2\phi_B)^{1.5}\right\}\right]$$

Drain current NMOS (weak inversion)

$$I_D = \frac{\mu_n W u_T}{L}\int_0^L \frac{dQ_n}{dx}dx = \frac{\mu_n W u_T}{L}Q_n = -\frac{\mu_n W u_T^2}{L}C_{dep}\exp\left(\frac{V_{GB} - \alpha\phi_B}{m \cdot u_T}\right)$$

Level 3 model (square law model)

$$I_D = \begin{cases} 0 & V_{GS} < V_T \\ \frac{KP}{2}\frac{W}{L_{eff}}(V_{GS} - V_T)^2 \cdot (1 + LAMBDA \cdot V_{DS}) & 0 < V_{GS} - V_T \le V_{DS} \\ \frac{KP}{2}\frac{W}{L_{eff}}V_{DS}(2(V_{GS} - V_T) - V_{DS})(1 + LAMBDA \cdot V_{DS}) & 0 < V_{DS} < V_{GS} - V_T \end{cases}$$

Capacitances in MOS

$$C_{GB} = C'_{GB}L_{eff}$$

$$C_{GS} = \frac{2}{3}C_{ox}WL_{eff}\left\{1 - \left(\frac{V_{GS} - V_{DS} - V_T}{2(V_{GS} - V_T) - V_{DS}}\right)^2\right\} + C'_{GS}W$$

$$C_{GD} = \frac{2}{3}C_{ox}WL_{eff}\left\{1 - \left(\frac{V_{GS} - V_T}{2(V_{GS} - V_T) - V_{DS}}\right)^2\right\} + C'_{GD}W$$

Small signal model

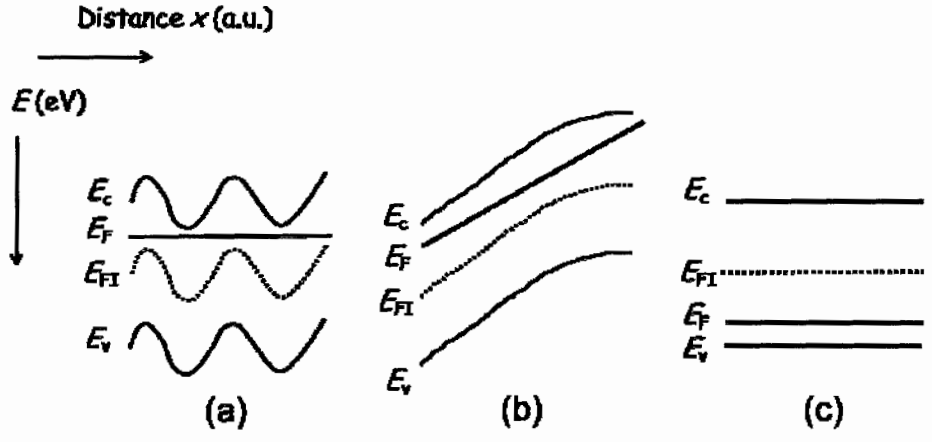
$$i_D = g_m v_{GS} + g_{ds} v_{DS} + g_{mbs} v_{BS}$$

Question 1, Semiconductor Physics

a) Consider two one-dimensional (1D) silicon structures which have been uniformly doped with the following concentrations:
structure 1: acceptor concentration=10^4 cm^{-3} and donor concentration=10^{15} cm^{-3}.
structure 2: acceptor concentration=10^{18} cm^{-3} and donor concentration=10^{18} cm^{-3}.
The structures are at thermal equilibrium (T=300 K) and we assume that the doping does not have any effect on the charge carrier mobility. Calculate the charge carrier concentrations and the conductivities of both structures. (Please note the physical units.) Explain which charge carriers determine the conductivity in each of the structures.

b) Please explain in words why extrinsic semiconductors become intrinsic for evaluated (ambient) temperatures. Now assume that for the effective densities-of-states in silicon holds that N_c=N_v=$5\cdot10^{19}$ cm^{-3} and the band gap E_g=1.1eV. The effective densities-of-states are assumed to be temperature independent. In case of an extrinsic semiconductor structure considered in a), determine the temperature at which the structure(s) become(s) intrinsic. (*Hint*: First check the relations for the charge carrier concentrations on the formula sheet and try to determine a function for $n_i(T)$ first. This you will need to solve the problem). Are the results in agreement with the expectations? Explain.

Consider the schematic energy band diagrams depicted below for different 1D semiconductor systems: (a), (b) and (c). The pictures are to the same (linear) scale.



Please answer the following questions.

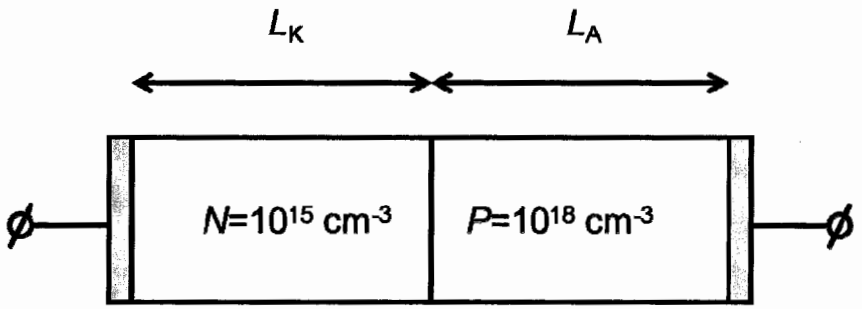
c) Explain in what system(s) there is a uniform doping distribution. Would that be then n-type or p-type doping?
d) In what system(s) we have the thermal equilibrium condition? Explain.
e) For what system(s) there is a uniform field distribution? Explain.
f) Please explain in what system(s) the external electric field is the highest.
g) For what system(s) there is a net current. What physical process (drift or diffusion) determines the current? Explain.

Rating: a) 30 b) 20 c) 10, d) 10, e) 10, f) 10, g) 10 points

Question 2, PN-junction

A schematic cross-section of a one-dimensional (1D) silicon pn-junction is depicted in the figure below. Both edges of the component have a metal contact.
For convenience sake we assume the following:

1. the diode operates at room temperature (T=300 K),
2. the doping concentration does not have any effect on the transport parameters such as the mobility and the bandgap,
3. the metal contacts of the component are "ohmic" (ideal),
4. and the depletion approximation is applicable here.



Further assume that the diode is at thermal equilibrium unless stated otherwise.

a) Sketch the space charge concentration against the distance. In what layer the depletion width W is mainly formed? Please explain.
b) Also sketch the electric field and the potential of the diode against the distance. Explain.
c) Calculate the built-in potential and the depletion width W. Also determine the maximum field.

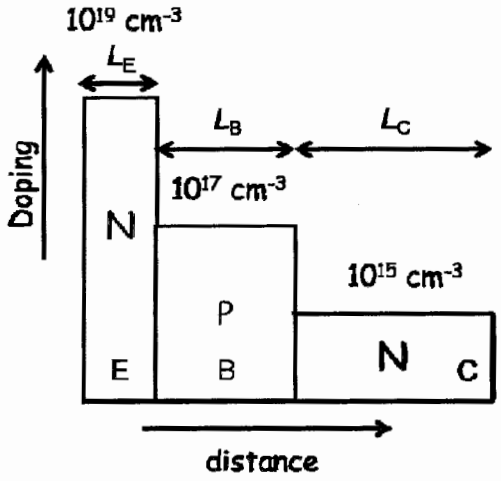
Assume that L_K=L_A and that both parameters (L_K, L_A) are much greater than the hole (L_p) respectively electron (L_n) diffusion length. Hence we have a long diode.
Now we apply an external potential of +0.5 V to the anode and 0V to the cathode.

d) Explain what charge carriers (holes, electrons) determine the total current of the diode. Are these minorities or majorities?
e) Sketch the hole-, electron-, and the total current densities (*i.e.* J_p, J_n and J) through the device as a function of the distance.

Rating: a) 10 b) 20 c) 30 d) 20 e) 20 points

Question 3, Bipolar Junction Transistor

Consider a one-dimensional (1D) silicon NPN bipolar junction transistor (BJT) with a doping profile as depicted below.



For convenience sake we assume the following:

1. the transistor operates at room temperature (T=300K),
2. the doping concentration does not affect the transport parameters such as the mobility and band gap,
3. the depletion approximation is valid to be used,
4. and the base current is only determined by the hole current.

a) Sketch the energy band diagram of the BJT at thermal equilibrium. Notice the doping concentrations. Please indicate carefully the following parameters: conduction band energy (E_C), valence band energy (E_V), intrinsic Fermi-level (E_{FI}), Fermi-level (E_F), depletion regions, emitter, base, collector.

b) We now operate the transistor in "forward active mode". Like in most semiconductor devices the potential barrier is important for the current flow. Please clearly indicate in the band diagram which you have drawn in a), what potential barrier, *i.e.* energy level difference, is important for the collector current, and likewise for the base current. Clearly describe what energy level difference(s) is (are) referred to. What impact will it have on this (these) barrier(s) when we increase the (positive) value of the base-emitter voltage V_{BE}?

Assume that L_B=1μm, L_E=0.5μm en L_C=2μm.

c) We operate the transistor at V_{BE}=0.5V and the collector-base voltage V_{CB}=0V. Calculate the collector current density J_C and the current gain β_F. Please write down clearly how you obtained the final results.

d) Typically, the doping profile of the BJT is asymmetric. In most cases, like in our device, the collector doping concentration is less than that of the emitter. Please come up with two reasons why this is the case and give an explanation for this.

e) Draw the large-signal equivalent circuit diagram of our bipolar transistor in common emitter mode.

Rating: a) 25 b) 15 c) 30 d) 10 e) 20 points

Question 4, MOS Transistor

Let's assume that the saturation current of conventional bulk MOS transistor can be described as (square law model):

$$I_D = \frac{\mu \cdot C_{ox} \cdot W}{2L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}), \quad \text{with}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}},$$

with L being the gate length. The substrate (or back gate) has been connected to the source contact.

a) Draw a schematic cross-section of an NMOS transistor and indicate in the figure what happens when the device is in saturation mode. Please explain.

In a microprocessor the so-called on-current $I_D=I_{on}$ at $V_{GS}=V_{DS}=V_{DD}$ (supply voltage) should be increased such that we also have more functionality and preferably a higher speed.

b) What do you think what should happen in the technology when the consumer would like to have both more functionality and an increased switching speed of the processor?

c) Describe at least two approaches to increase the current and explain what will be their limit for a proper functioning of the NMOS. Please come up with a possible solution for postponing or to get rid of these limits.

d) Draw a small-signal equivalent circuit diagram of our NMOS in common-source mode.

e) Give a mathematical description for the transconductance g_m assuming the model described above.

f) Give a mathematical description for the conductance g_d at saturation mode assuming the model described above. For a circuit designer the (output) conductance should be minimized preferably to zero A/V. Please describe in words what should be done in the technology to obtain a zero output conductance.

Rating: a) 20, b) 5, c) 20, d) 30, e) 10, f) 15 points