Module 11 Electronic System Design 201500383, Test ESP-Analog Signal Processing

Date : Tuesday March 8, 2016
Venue : Therm
Time : 08:45 – 11:45 (90 minutes for this test)

Rules:

- All Answers must be clarified
- This test is "open book": Lecture notes, personal notes, hardcopies of slides may be used.
- It is permitted to use a simple calculator
- It is not permitted to use mobile phones or other communication devices

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Exercise 1 (total: 25 points)

In a harddisk system the bits are stored in the magnetic domain. The bits are being read out by a reading head, and the signal coming from the reading head is amplified by a broad-band amplifier. The signal of interest lays in the frequency band from 10MHz to 1GHz. However besides the pure bits, it also contains a lot of disturbing signals. We want to process the signal in the digital domain to obtain the clean data bits. For this purpose, we need to digitize the output signal from the broad band amplifier. This signal has a magnitude of $200mV_{RMS}$ and is directly connected to the AD Converter because the signal exactly "fits" into the input voltage window of the ADC.

a) (1) What should be the minimal sample rate of the ADC if we want to capture the signal in the digital domain?

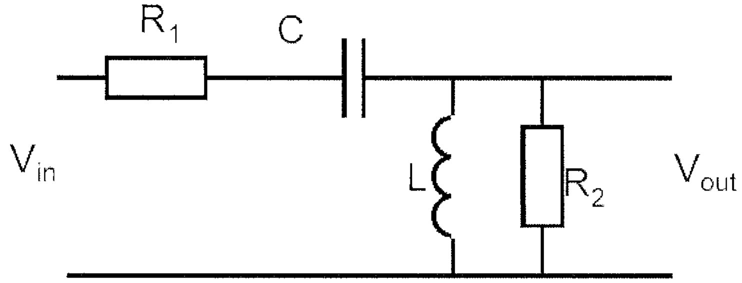
b) (1) The signal of interest has a signal-to-noise ratio of 33dB. How many bits must the ADC have? And what type of ADC would you choose?

c) (2) The FoM (Figure of Merit) of the ADC is 0,5pJ/conversion. Give an estimation of the power dissipation of the ADC.

Now there appears to be a problem: The motor drive circuit makes an interfering signal of $1V_{RMS}$ at a frequency of 100KHz at the input of the ADC. In order to still be able to capture the signal with a signal-to-noise ratio of 33dB we determine to change the ADC.

d) (3) What specification points of the ADC should be changed? Give an estimation of the new power dissipation if the FoM (Figure of Merit) of the ADC remains 0,5pJ/conversion

We decide to filter out the 100kHz signal with an analog filter in front of the ADC. This way we do not have to change the ADC so much and we can safe power in the ADC. The filter is placed between the output of the broadband amplifier and the ADC input.



We want to integrate this filter on the same IC as the amplifier and the ADC. Because it's hard to integrate inductors of good quality, we have to make an active implementation of the filter.

e) (1) which realization form (Opamp-RC or gm-C) has your preference? Please motivate your choice.

f) (1) This second order high pass filter cannot easily be described with the standard state-space equations. How can you still design this filter in an active form?

g) (5) give the active realization of this filter and express all component values in R_1 R_2 L en C.

h) (3) now it appears that the noise of the filter is 4 dB too large. How can you redesign the filter in such a way that it satisfies the noise specification again? What are the new component values, expressed in the old values?

i) (3) Give an expression of the power dissipation of the new filter (under h) compared to the old filter (under g)

j) (5) Now there appears to be a small but nasty disturbing signal of $10mV_{rms}$ at 3GHz at the input of the ADC. What is according to you the best way to change the system to deal with this? You can change both the analog part and/or do something in the digital domain. Give a motivation and also the necessary details. Please keep in mind the over all power consumption and the simplicity of the system.

--- end of exercise 1 --

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Exercise 1. FFT [8 points]
In a hardware application a DFT of length N must be computed, but the only available hardware can do an FFT of length kN for some $k \in \mathbb{N}$ and $k > 1$.

1. [**4 points**] Explain how this hardware can be applied to compute the N-point DFT.
2. [**4 points**] Assume that the number of complex operations for computing an M-point FFT is $M \log_2(M)$. Take $N = 128$ and $k = 2^r$, $r \in \mathbb{N}$. What is the maximum r for which it would be beneficial in terms of computational complexity to use the available FFT hardware instead of a direct implementation? Count the combination of an complex multiplication and an addition as *one* complex operation.

Exercise 2. Spectral DSP [8 points]
Study Figure 1 on Page 3, representing a block diagram of overlap-add filtering in the DFT domain. The segment length that is processed is N. The length of the DFT is M. The filter length is K.

1. [**4 points**] What is the minimum value of M for proper operation?

2. **[4 points]** In the right-hand side of the diagram, where the output signal is reconstructed, which adders *must* be implemented as adders and which do not have to be?

Exercise 3. Sampling-rate conversion [5 points]
A two-stage down-sampling system with a total decimation factor $D = D_1 D_2 = 20$ is realised in 2 stages, one with a decimation factor 4 and one with a decimation factor 5. The decimation factor of the first stage (at the input side) is D_1. The decimation factor at the last stage is D_2.

1. **[3 points]** What is the best choice of D_1 and D_2 for the most computationally efficient realisation?
2. **[3 points]** What are the transition bands of the lowpass filters of Stage 1 and Stage 2, expressed on the normalised (positive) frequency scale $[0, \pi)$.

Exercise 4. 2D DSP [3 points]
For the 2D impulse response $h[m,n]$ we have that $h[m,n] \leftrightarrow \mathcal{H}(e^{j\Psi}, e^{j\Omega})$, and $h[m,n] = f[m]g[n]$, with $f[m] \leftrightarrow \mathcal{F}(e^{j\Psi})$ and $g[n] \leftrightarrow \mathcal{G}(e^{j\Omega})$. Prove that

$$\mathcal{H}(e^{j\Psi}, e^{j\Omega}) = \mathcal{F}(e^{j\Psi})\mathcal{G}(e^{j\Omega}).$$

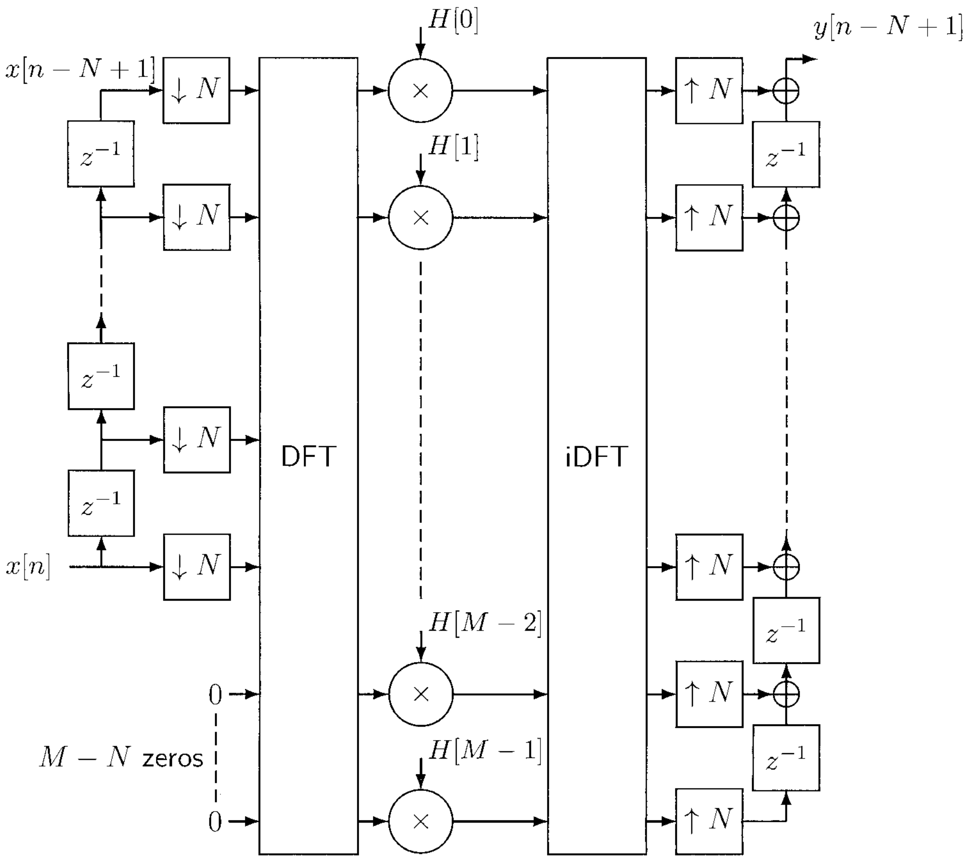

Figure 1: *Block diagram of overlap-add filtering in the DFT domain.*