Joint Exam "Technology" (191210730) and "Fabrication of nanostructures" (201600042)
January 18th, 2021

General instructions: see the info on the previous page.

Part II: Answering questions (1-6) of the exam (55 points max).

Question 1. True or False? Shortly motivate each answer (1 point each, 10 points max).

1) SiO_2-to-Si interface is not the best in terms of interface states, GeO_2-to-Ge behaves better.
2) Growing GaN epitaxially on (111) Si wafers requires an extra thin buffer layer in between.
3) Substrate gettering is not required if devices are processed in the best-class clean rooms.
4) Rapid thermal annealing is often applied to enhance long-range diffusion of dopants.
5) Materials utilized as diffusion barriers should exhibit a lower activation energy for diffusion.
6) Oxidation of silicon starts with a parabolic regime and continues with a linear regime.
7) Proximity printing in optical lithography is related to the photoresist-exposure proximity effect.
8) Applying magnetic fields to plasma helps to decelerate energetic ions and neutral species.
9) Controlling substrate temperature is not crucial for deep reactive ion etching.
10) PEALD has a better step coverage than thermal ALD.

Question 2: Epitaxy (10 points max)

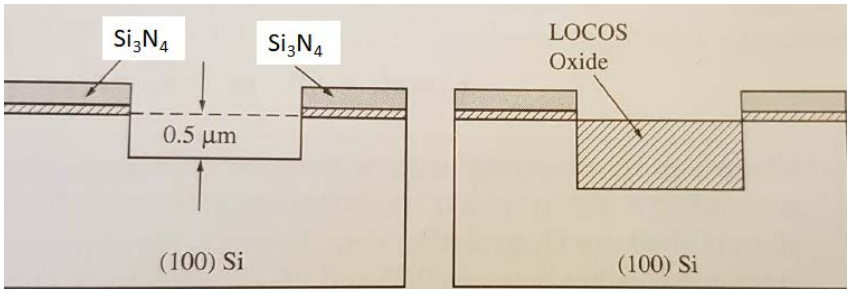
Growth rates as a function of temperature are given on the right for Si epitaxy from SiH_4.

700	750	800	850	900
0.04	0.09	0.2	0.4	0.5
950	1000	1050	1100 °C	
0.6	0.7	0.75	0.8 μm/min	

a) Make the corresponding Arrhenius graph. (3 points)
b) Explain the occurrence of the two regimes that you observe in the Arrhenius graph. (2 points)
c) Calculate the averaged activation energy of chemical reactions, explaining all the steps behind. (5 points)

Question 3. Oxidation (10 points max).

a) For the left structure shown on the right, with 500 nm of Si etched prior to the oxidation at 1 Atm total pressure, calculate how long (in hours or minutes) must the wafer be oxidized at 1000 °C in H_2O to produce the planar oxide completely filling the etched-in-the-Si cavity (see the most right picture). Use the data provided in table 6-2 below, not forgetting that Si is being consumed during oxidation. (7 points)



b) What would happen if the Si_3N_4 layer was not present? Draw the corresponding oxidation profile (on scale, indicating Si/SiO_2 interface position in all areas) next to image on the right. (3 points)

Table 6–2 Rate constants describing (111) silicon oxidation kinetics at 1 Atm total pressure. For the corresponding values for (100) silicon, all C_2 values should be divided by 1.68.

Ambient	*B*	*B/A*
Dry O_2	$C_1 = 7.72 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 6.23 \times 10^6\ \mu m\ hr^{-1}$
	$E_1 = 1.23$ eV	$E_2 = 2.0$ eV
Wet O_2	$C_1 = 2.14 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 8.95 \times 10^7\ \mu m\ hr^{-1}$
	$E_1 = 0.71$ eV	$E_2 = 2.05$ eV
H_2O	$C_1 = 3.86 \times 10^2\ \mu m^2\ hr^{-1}$	$C_2 = 1.63 \times 10^8\ \mu m\ hr^{-1}$
	$E_1 = 0.78$ eV	$E_2 = 2.05$ eV

Question 4. Lithography (10 points max).

a) Calculate and plot (on scale) versus the six (g-line, i-line, KrF, ArF, F_2, Ar_2) exposure wavelength the theoretical resolution and depth of focus for a projection system with a numerical aperture of 0.8 and k_1=0.55 and k_2=0.7. Indicate the wavelength sources on the graph. (3 points)

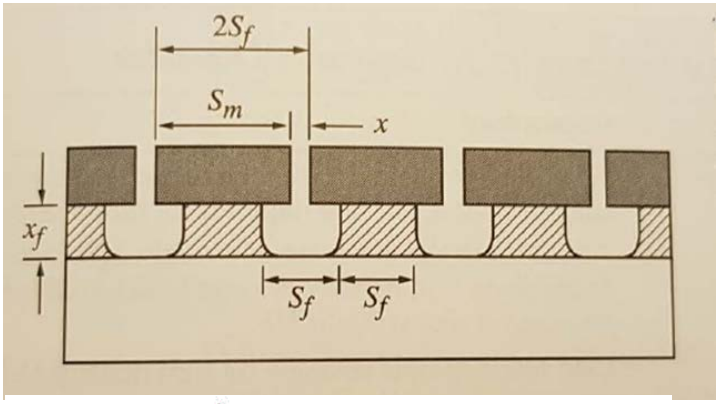
b) Which source(s) would you propose for the 180-nm technology generation and why? (1 point) What would be the maximum photoresist thickness that you can apply and why? (1 point)

c) Which practical solutions lead to achieving a 35-nm resolution with the 193-nm source? (3 points)

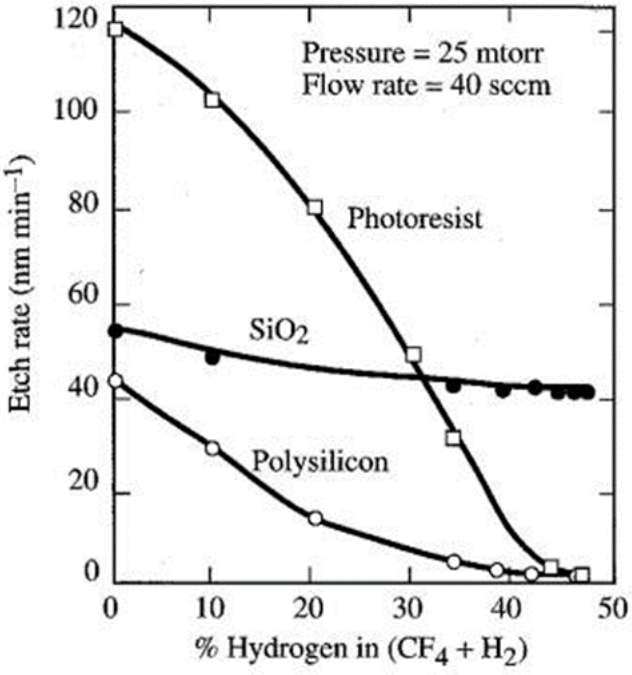
d) Sometimes it is difficult to develop away the last few nanometers of photoresist in certain exposed areas. Suggest a possible cause of this problem and propose a solution. (2 points)

Question 5: Etching (10 points max).

a) Consider the structure shown on the right-hand side. The gray-square blocks on top correspond to photoresist. A 0.5-um-thick SiO_2 layer below is etched with a degree of anisotropy of 0.8. The distance between the mask edges, *x*, is 0.35 um. Calculate (i) the undercut and (ii) final width of the remaining oxide blocks. (2 points)

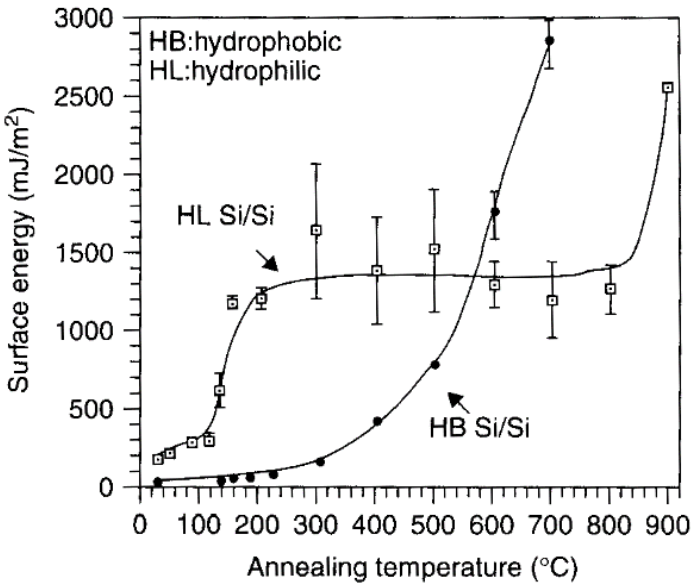


b) Consider the graph shown on the right-hand side. A 0.5-um layer of silicon dioxide on a Si substrate needs to be etched down (patterned) to the Si in a plasma containing 30% of H_2 in CF_4/H_2 mixture. There is a ± 5% variation in the oxide thickness and ± 5% variation in the oxide etch rate. Calculate (i) the minimal etch time ensuring that all the oxide is removed (2 points), (ii) the thickness of poly-Si that has been etched as a result of overetching the oxide (2 points), (iii) minimal thickness of the photoresist required to safely protect the oxide which is not supposed to be etched (2 points), and (iv) thickness of the remaining oxide if changing the recipe to 50% of H_2 in CF_4/H_2 mixture, while keeping the minimal etch time of (i) unchanged (2 points). The required data can be taken from the graph on the right.



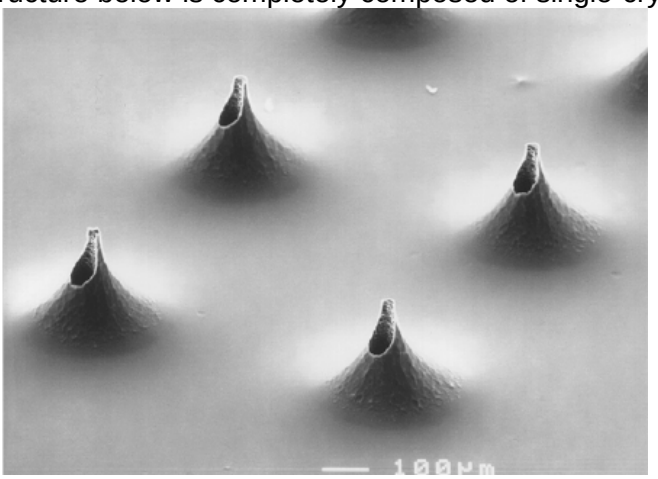
Question 6: Unknown graph (5 points max).

Explain the graph on the right by shortly answering the following questions. (i) Which field does it come from? (ii) The mentioned surface energy – this is a measure of what? (iii) What is the main cause of the difference between the two curves? (iv) What in you opinion is behind the existence of the long horizontal region for one of the curves? (v) Which of the two curves would you prefer if the process temperature cannot be increased beyond 400 °C and why?

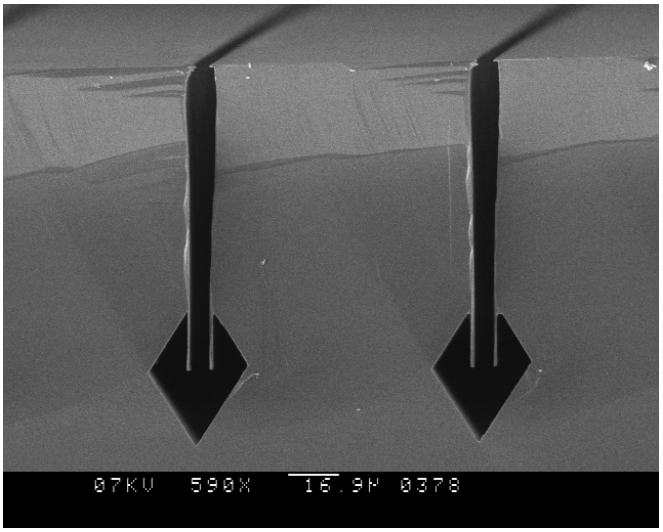


<u>Part III: 1st Question of choice (15 pts max). Choose only *one* question (i.e. 7, 8 or 9) to answer.</u>
Question 7: Silicon microtechnology with applications in energy and chemistry (15 points max).
Below you see 3 pictures of micro or nano structures made with silicon-based micromachining methods. Please explain with which method(s) these structures were fabricated (best is to make schematic drawings). Make a schematic drawing of the design of the photolithographic mask(s) that can be applied to make these structures. Also indicate which masking layers could be used, and explain why the shapes have become like those shown in the images. If the structure is composed of different materials, explain how they were connected to each other. For each part (i.e. (a), (b) and (c)) you can be awarded 5 points.

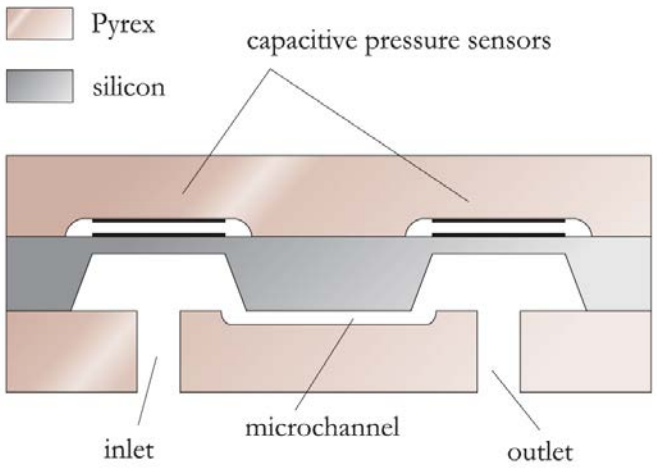
(a) Extra information: the structure below is completely composed of single-crystalline silicon.



(b) Extra information for the structure below: the substrate is single-crystalline silicon; the image shows a cross-section of the substrate.



(c) Extra information: the image below shows a cross-sectional view of two pressure sensors which are connected at both ends of a microchannel (in this way one can measure the viscosity of the fluid, if the flow rate is fixed and known). The black lines in the top glass plate are the metal electrodes. In your answer, you can neglect the inlet and outlet holes in the lower glass plate, these were made by drilling.



Question 8. Sensors (15 points max).
Heating and temperature sensing is important for many applications, e.g. for flow meters and for Wobbe index meters.

(a) How can we make heaters and temperature sensors on top of (1) a flat surface silicon substrate, or (2) a flow tube made with the surface channel technology? (2 points)
(b) Why are thermopiles preferred over resistors as temperature sensors? Which features of thermopiles are important, and why? (2 points)

Single side heating limits the amount of heat that can be provided to the flow or combustion process.
(c) How can we supply heat from more than 1 side? With which technology can this type of heaters be made? How could we fabricate a heater at the bottom of a flow tube? (3 points)

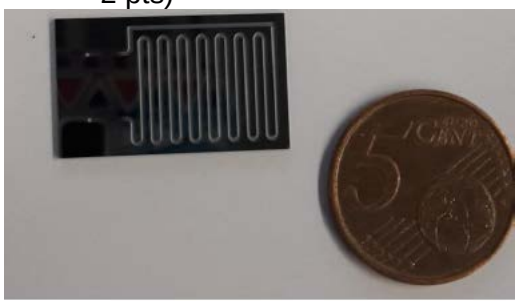
We can make several sensing structures in the surface channel technology.
(d) Which types of devices / sensors can be made with the surface channel technology (mention at least 4 different sensors)? Which additional features can we achieve by combining these devices / sensors? (2 points)
(e) Describe the main fabrication steps when making a Coriolis flow sensor with the surface channel technology. Why is it beneficial to use the surface channel technology over bulk micromachining? How should the process be modified to make a thermal flow sensor? (4 points)

The surface channel technology has a limitation in the maximum flow channel diameter of ca. 100 micron. Furthermore, the cross-section of the flow channel is not perfectly circular.
(f) How can we make flow channels with bigger diameters, e.g. 400 microns? How can we make more circular flow channels ? (2 points)

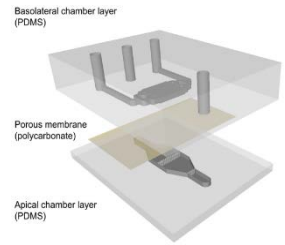
Question 9. LOC technology (15 points max).

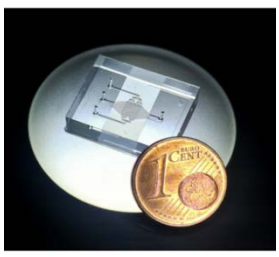
a) 3D printing has recently been introduced in the field of microfluidics, as an alternative fabrication approach. What are the motivations to use 3D printing instead of conventional fabrication approaches (1 point)? A researcher would like to quickly test an idea of design for a microfluidic device (the nature of the material does not matter for this quick test):
   a. Would you advise him/her to use 3D printing or to rather use a more conventional fabrication route? ***Explain***. (2 pts)
   b. One key element in this design has features with dimensions of less than 10 micrometers. Is there a 3D printing technique you would recommend this researcher to use to produce his/her targeted design? ***Explain***. (2 pts)
   c. Explain why most 3D printing techniques produce rough structures. (2 pts)

b) Considering the microfluidic features presented below, propose a possible and complete fabrication process ***from the design to the final assembled structures***. (8 pts = 3 pts + 3 pts + 2 pts)

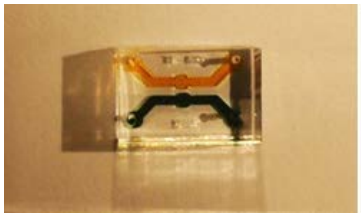


i) Silicon-glass device (*picture on the left side*), knowing that:
- microfluidic structures are created in the silicon substrate and have a **rectangular** cross-section,
- reservoirs machined in the silicon substrate.
Source : Ripken et al., 2019.





ii) PDMS-membrane-PDMS microdevice (*cartoon on the left side*), knowing that:
- the device comprises three layers, with two fluidic PDMS layers sandwiching a polycarbonate porous membrane;
- both PDMS layers house a chamber and inlet and outlet channels;
- all microfluidic structures are 350 µm in height.
Source : Ferraz et al., Nat. Comm., 2018.



iii) PDMS-glass device (*picture on the left side*), knowing that :
- microfluidic structures (*picture on the right side*) and reservoirs are in PDMS ;
- the height of the microfluidic structures is 500 microns.

Part IV: 2nd Question of choice (15 points max). Choose only *one* question (10 or 11) to answer.

Question 10. ICs & LEDs (15 points max).

CMOS technology (9 points).

a) Put these fabrication steps in the right order for CMOS:
spacers - isolation – contacts – metal 1 – gate – silicide. (2 points)

b) For each of these six steps, specify if an insulator, a semiconductor or a conductor is added. (1 pt)

c) To make CMOS, we need to fabricate NMOS and PMOS transistors on the same wafer. Describe the technological disadvantages and problems that follow from this combination, compared to a process that only produces NMOS or PMOS transistors on a wafer. (Hint: what do we need to do extra?) (4 points)

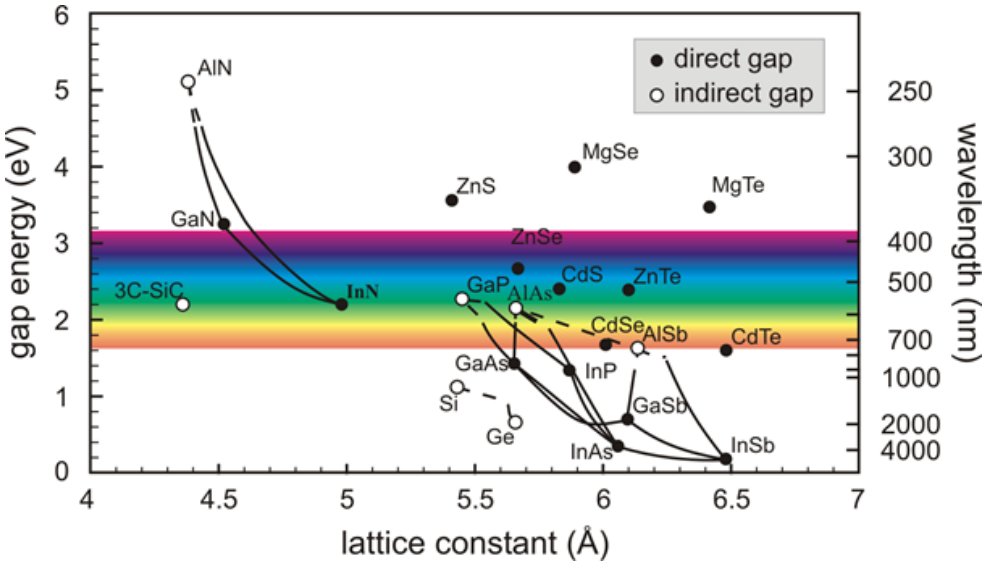
d) We use relatively thick photoresist for the well implantations, about 2-3 micrometer. Why? (2 points)

Light-emitting diodes (6 points)

e) Of the many inventors involved in LED technology development since the 1960s, a Nobel Prize was awarded only to Nakamura, Akasaki and Amano. What distinguishes their work from the other LED inventors, motivating the Nobel Prize committee's choice? (More than one answer possible.) (2 points)

f) Describe the purpose of heterojunctions in LEDs. (2 points)

g) See the picture below. Explain why the lattice constant is an important consideration in LED technology. (2 points)



Question 11. NanoElectronics (15 points max).

a) Make a schematic drawing of a simple neural network and indicate its main characteristics. (3 points)

b) Describe the concept "Evolution in Materio" in a few sentences. (4 points)

c) Give at least two advantages, and also at least two disadvantages, of the application of this concept to the development of hardware for machine learning. Motivate your statements. (4 points)

d) Why is the operation temperature of the nanodevices based on dopant networks in silicon much higher than that of nanodevices based on gold nanoparticle networks? Motivate your answer. (4 points)

END OF EXAM