# Exam IC Technology 2005

General comments
This exam comprises 3 questions with equal weight for the final mark. The students are allowed 3 hours for answering. No books, calculators or handouts are allowed.

For students using this exam as preparation:
The questions asked in this test are representative of the type of questions I may ask during upcoming exams. Normally I don't ask a lot of "calculation" questions, but rather I focus on knowledge, understanding and interpretation. (An example of the latter is question 3 in this example exam.)
This exam was used in 2005, when we still used a different book (Campbell) and the lectures were of course a bit different than today.

As a final note: this example exam has no questions about isolation, CMOS or memories, but in general, you can expect questions about all topics covered in the course.

**Question 1: Backend technology**

The specific contact resistance between Al and n+ silicon is $4.10^{-6}$ $\Omega.cm^2$. (Sheet 5 of Back end II).

a) compute the resistance of an Al/n+ Si contact with a diameter of 1.13 µm.

Answer: The area is ¼ $\pi D^2$ = 1,003 $\mu m^2$ so R = $4.10^{-6}$ $\Omega.cm^2$ / 1,003 $\mu m^2$ = 400 $\Omega$. Score: 30 points max.

b) Why do we observe much higher contact resistances in this type of contact when Al(1%Si) is used?

Answer: At a deposition temperature of around 400 C, the solubility of silicon in aluminum is limited to 0,5% and at room temperature the solubility is virtually zero Therefore, there is too much silicon in this mixture and the silicon will precipitate (form clusters). Silicon clusters will cover the doped Si contact area and they have a much lower conductivity than aluminum and therefore the overall resistance will go up. (Campbell page 420.) Score: 50 points.
*The answer that this AlSi compound reduces junction spiking, and therefore reduces the effective contact area between Al and Si, has been honored with 25 points.*

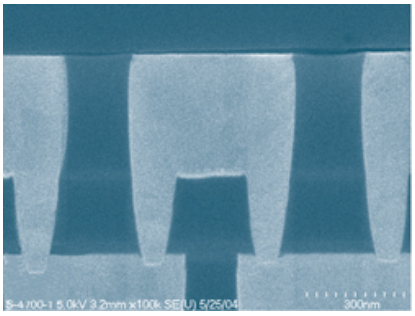
c) The specific contact resistance of self-aligned $TiSi_2$ towards $n^+Si$ is much lower: $2.10^{-7}$ $\Omega.cm^2$. Give at least one good reason why this is so.

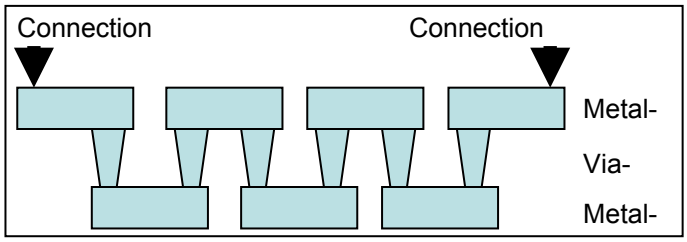
Answer:
1. There is no ($p^-$ doped) Si on top of the n+ doped Si
2. Due to the $TiSi_2$ formation the Si-$TiSi_2$ interface is extremely clean.
3. At the formation of $TiSi_2$ there will be an accumulation of dopant in the Si at the Si-$TiSi_2$ interface, giving rise to lower contact resistance. Score: 60 points.

d) The resistance of an Al/Ti-TiN-W contact with 0.5 µm diameter is around 1 Ω. (Sheet 47/53 of Back end I). Why is this resistance so much lower?

Answer: This is not a metal-semiconductor contact, but a metal-metal contact. There is no exponential dependence on metal-semiconductor barrier height and dopant concentration ($\Phi_B/N_D^{1/2}$). The contact resistance is mainly determined by the cleanliness of the interfaces. Score: 60 points.
*This question was not understood by the students, judging from their answers. It was discarded from the final score.*

A so-called via string (or via *chain*) is fabricated to assess the yield of vias in a modern IC process. Below are a cross-section picture and a sketch of the organization of such a test structure. It is meant to verify the quality of the processing, and it is not part of a normal integrated circuit.






e) Is the structure in the left figure fabricated with conventional, single-damascene, or dual-damascene processing? (Motivate your answer.)

Answer: Dual-damascene. The vias and the metal above it are clearly deposited in one step (there is no interface visible). Conventional technology and single-damascene technology both require that the via is first formed, and the metallization is later deposited on top. Also, there is clearly no overlap of metal over via, which is not well manufacturable when conventional or single-damascene processing is used. Score: 50 points (only when motivation is really good.)

f) Make an order-of-magnitude estimate of the number of contacts and vias in a Pentium-IV processor. To verify if the via yield is high enough for making these Pentium processors, how many vias should be included in the test structure?

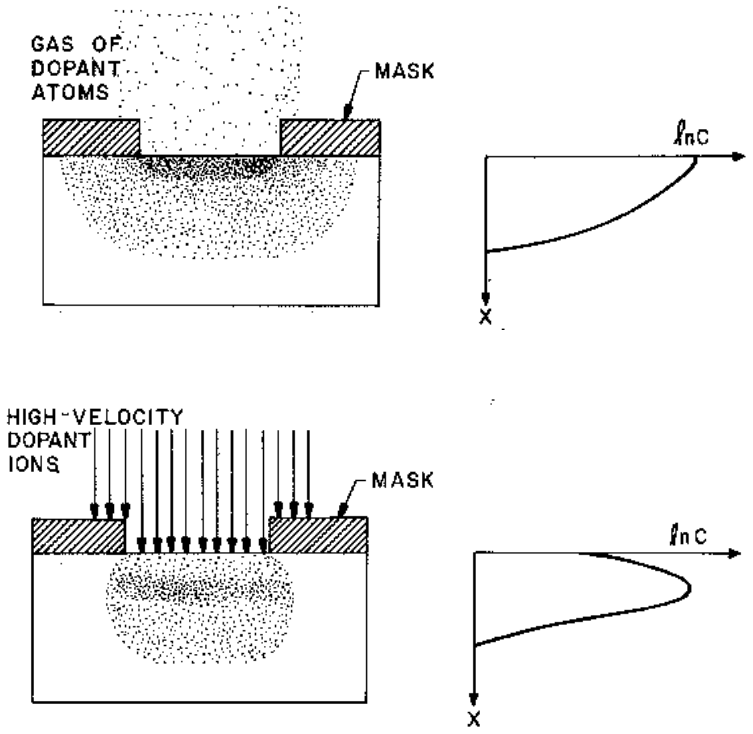
Answer: There's about a hundred million transistors on a Pentium-IV chip. Each transistor is a 4-terminal device so the maximum amount of contacts for such a chip would be 400 million[1]. There will never be as many vias (per via level) as contacts, because the design rules are more relaxed for higher levels. A billion vias would be a nice estimate of the number of vias in a Pentium-IV.
A test structure should allow us to quantify a yield number between 0% and 90% for this amount of contacts and vias. That means that the test structure should also have several hundred million contacts and vias. Not very convenient! It is perhaps easier to make the Pentium and find out if it works. Score: 30 points.

g) Based on your answer in question f and an educated estimate of the resistance of one of these vias, make a proposal how to measure whether the contacts are making good contact. (Hint: keep in mind the following considerations: how much voltage would be safely put onto such a test structure in a planar technology? How much current can you measure accurately? How much current is safely driven through such a structure? And how will you decide whether the structure is good or bad?)

Answer: The answer depends strongly on the result from question f. Given that you cannot use much more than 5 V, and that each contact or via has 1 Ω resistance, we should be able to measure 1 nA current when 5 billion contacts

[1] In digital electronics the number of contacts is typically 1-2 per transistors.

and vias are chained. This is easy to do, currents above 1 pA are easily measured. Of course this amount of current can be easily coped with by all elements in the measurement chain, including the test structure components themselves.
To decide between bad and good test structures (for yield assessment), a fixed voltage can be applied and the current measured. When the current is (within certain bounds) close to the expected current, the test structure is said to be OK: when the current is not too far off the “1 nA” this implies that all contacts are normal. When one contact is missing, no current will flow whatsoever. Typically the current meter will still give a value, around 1 pA or so, simply because it always has some drift so it is not very good at measuring 0. Score: 30 points.




**Question 2: impurities in silicon**

The figure above comes from one of the fist slides used in the lectures. It shows two methods of "contaminating" silicon with impurities.

a) How are these techniques called?

Answer: The upper one is called diffusion, the lower is (ion) implantation. 20 points each.

b) Explain briefly how they work and what are typical process conditions (e.g. indicate roughly the temperature, ambient pressure, time spent in the machine).

Answer: How they work: a good explanation for both can be found in Campbell (30 points maximum for diffusion, 30 points max for implantation, including an explanation of mass separation). Diffusion: 800-1000 C, a few mTorr to 1 atm, typically 15 minutes to 2 hours. Implantation: normally at room temperature (although the wafer can get hot when the ion implantation is done with a high-current implanter; and in some peculiar cases, the wafers are cooled down to -60 C or so), under high vacuum, typically a few minutes per wafer. (5 points for good indication of each of these six process conditions.) Total: 90 points max.

c) Explain how in each case the mask prevents the impurities from getting into the silicon. What typical materials could be used as a mask here?

Answer: For diffusion, it is imperative that the mask prevents impurities from moving through the mask into the silicon. This can be achieved in two ways (!):

either the diffusion constant in the mask material is very low, or the solubility limit in the mask material is very low. 20 points each.
For Ion implantation, the stopping power of the mask material counts: the mask should bring the implanted ions to a full halt before they get into the silicon. 40 points.
Masking materials include materials that are silicon technology compatible and that can be selectively removed again later. For diffusion, SiO2 and Si3N4 are good. For implantation, these also work, and poly (on top of thin SiO2) and photoresist can also be used. 20 points overall for a good answer to this question (at least two good materials and no errors made).
Total: 20+20+40+20 = 100 max.

d) The upper technique was used a lot in old IC processes, the lower one in newer processes. Explain why this is so.

Answer: Diffusion is *cheap* and simple (2*10 points). It also happened to be the first method people found to be rather reproducible. (The students may or may not remember this; it was part of the lectures of Technology.)
Ion implantation is more reproducible (10 points), gives less lateral extension (10 points) and allows for vertical profile tuning (10 points) whereas the profile of an indiffused impurity is more or less fixed in depth. It is also more expensive (already valued with 10 points earlier). It is also convenient that we can use photoresist as a mask, but I never discussed this so perhaps nobody comes up with it.
Total: 50 max.

e) With the second technique, the upper few nanometers of the silicon become contaminated with various elements other than silicon and the 'planned' impurity. Explain how this happens, and which elements one could expect to find in the upper nanometers.

Answer: The ion beam can 'sputter" material from the mask. The sputtered atoms or ions mostly have a lower energy than the original ions. This is why they do not get very deep when they hit the silicon after being sputtered off the mask. The ion beam can also sputter part of the implant system, in particular the material from the source chamber and shutters (diaphragms) in the beam line. Metals, oxygen, carbon and hydrogen can be found in the upper few nanometers. 50 points max.

**Question 3: integrated solenoid**

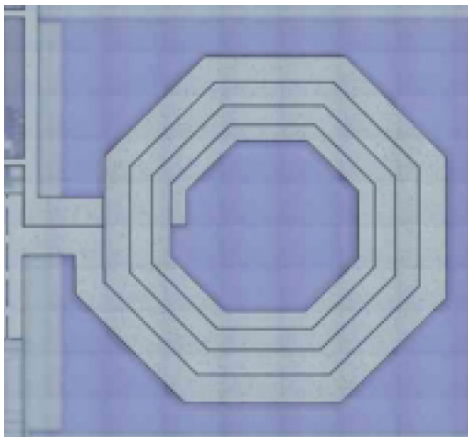
The figures below show photographs and sketches of a solenoid inductor structure, fabricated in planar technology. It was published in IEEE Electron Device Letters in March 2005 by Lin et al.

a) Inductors made in planar technology normally have a rather low quality factor *Q*, below 10. Explain what the quality factor is, and why it is low compared to that of lumped discrete inductors.

Answer: The quality factor expresses the ratio of the inductance L to the impedance of the parasitics. (40 points) A high quality factor means that the inductance is predominant over the parasitic components and that it can be treated as an ideal lumped element. It is low because the resistance of IC wires is relatively large (10 points), the shape of a planar inductor is not ideal (10 points), and eddy currents are created in the substrate (20 points). Score: 80 points max.

b) Make a sketch how inductors are usually made in an IC process. (The figure below is not typical!)

Answer: See the handouts. One typical example is shown below. Score: 80 points max. when also a cross section is drawn that shows how we use many layers of metal short-circuited with contacts. The drawings should be clear and explained, subtract points for unclear drawing.



c) The use of contacts in the current path of the inductor is necessary in the design below. Why is this a disadvantage?

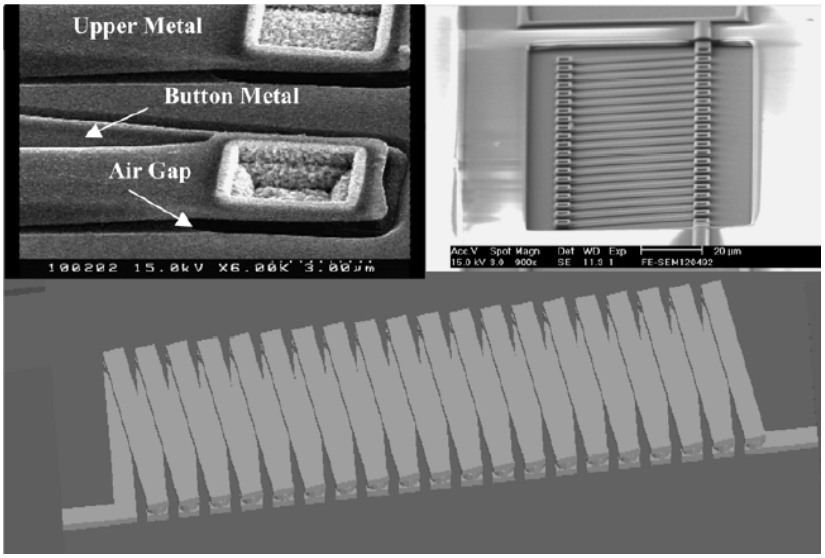
Answer: Because contacts have a high resistance compared to the same length of interconnect. So the internal resistance will be high leading to a lower quality factor. Score: 50 points max.

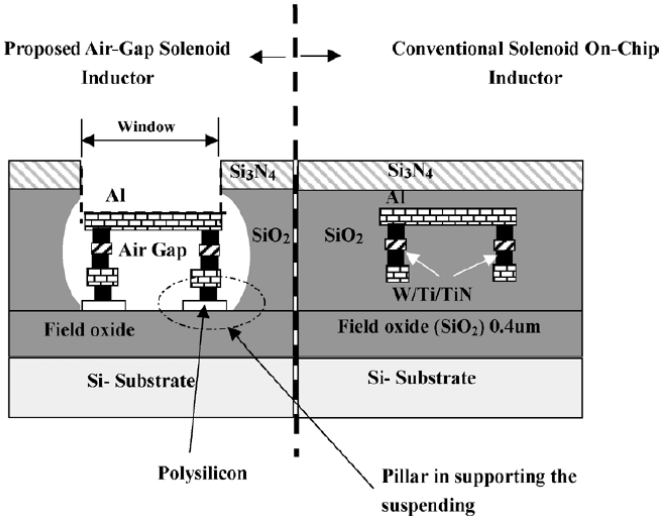
d) Why would a solenoid be an attractive alternative for the normal integrated inductor? (More than one answer is possible.)

Answer: The authors of the paper claim that the magnetic field will not penetrate the silicon as much, leading to less substrate loss (and therefore a higher quality factor). Also they claim that they can lay out an inductor using less silicon area in this manner. (Score: if one of the two is mentioned and no errors are made: 50 points max.)

e) (BONUS) In this case, an air gap was created around the solenoid. Explain how this can be done. What kind of complications can one expect when air gaps are formed in an integrated circuit? (More than one answer is possible.)

Answer: A selective etch must be used after opening of the Si3N4 layer shown in the cross section (20 bonus points). The selective etch should not etch the metals used for contact, via and interconnect, but should etch the SiO2. Funny in the sketch is that it appears to stop etching on the field oxide. This is a drawing mistake of the authors.
The suspended coil in the hole is vulnerable (more vulnerable than the rest of the chip) in the packaging process. When the wafers are diced, dust can get into this hole, creating e.g. short circuits or a lifetime problem. (10 points)
The quality factor depends on whether there is material inside the solenoid or not. (The students can understand this because otherwise there would be no reason to etch it free.) But after this process step, the chip will be mounted and after putting the bond wires in place, a plastic compound is used to seal the chip. This compound may get into the hole of the solenoid, damaging it or changing the quality factor by its presence (10 points).
Score: 40 max.




Proposed Air-Gap Solenoid Inductor
Conventional Solenoid On-Chip Inductor
Window
Si3N4
Si3N4
Al
Al
Air Gap
SiO2
SiO2
W/Ti/TiN
Field oxide
Field oxide (SiO2) 0.4um
Si- Substrate
Si- Substrate
Polysilicon
Pillar in supporting the suspending